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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,315	11/24/2003	Hirokazu Matsuura	FUSA 20.757	4295

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EXAMINER	
NAMAZI, MEHDI	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,315	MATSUURA ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to Request for Continued Examination (RCE) filed January 18, 2007.

Response to Arguments

Applicant's arguments filed on January 18, 2007 have been fully considered but they are not persuasive.

Applicant's arguments that "Again, Lin only includes a plain recognition that stale cached data needs to be replaced. And the cited portions of Lin only include description of "conventional logic" to monitor only "the write signal transferred on the control lines 250 to detect when information is to be changed within any of the slave devices 214 and 216 (Fig. 4)." Col. 5, lines 45-48 of Lin. If the data is cached, then the cache is "invalidated." Please see, e.g., col. 5, lines 65-66 of Lin has been considered. However Lin teaches a multiprocessor system wherein each processor has its own storage (cache) (figs. 5, and 6), and bus snooping (monitoring) for cache coherency in order to maintain coherency (having the same data and other informations) between information stored in the shared memory and copies of the information stored in one or more cache memories (col. 1, lines 34-36).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 6, and 9 recites the limitation "said address" in line 12, 11, and 11 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, and further in view of Lin (US. Patent No. 6,622,216).

As per claims 1, 6, and 9, AAPA teaches a multiprocessor system comprising a common memory and a number of processors connected via a common bus (fig. 10, processors elements 21, common memory 23, and G bus 10 which serving as common bus), only one processor being allowed to access the same data area of said common memory wherein (page 2, lines 26-27 "a prescribed processor is to acquire the bus-use privilege"); said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use (fig. 10 common memory 23 has been divided into plurality of data storage sections and a control information area "semf" for storing control information);

As per claims 1, 6, and 9, AAPA teaches the claimed invention, but fails to teach each processor is provided with a storage unit for storing same data and same control

information as those stored in the common memory and with an access controller; and the access controller of a processor monitors data and addresses that flow on the common bus, accepts data written to said common memory and data read from said common memory and stores this data in a memory area, which is designated by said address, of the storage unit within its own processor.

Lin teaches multiprocessor system wherein each processor has its own storage (cache) (figs. 5, and 6), and bus snooping (monitoring) for cache coherency in order to maintain coherency (having the same data and other informations) between information stored in the shared memory and copies of the information stored in one or more cache memories (col. 1, lines 34-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention to modify the work of AAPA, because Lin teaches bus snooping for cache coherency in order to maintain coherency between information stored in the shared memory and copies of the information stored in one or more cache memories (col. 1, lines 34-36).

As per claims 2, and 7, AAPA teaches identical addresses are allocated to address spaces of the storage unit of each processor and of the common memory (page 6, lines 5-40, controller 22 sends the read access to the common bus 10 and waits for common memory card CM to send back the result of acquisition of semf-a, if the semf-a is in use by CPU #0 than it sends back a signal that it is busy by another processor), and the access controller of the processor that does not have access

privilege writes data on the common bus to a storage area of a storage unit designed by an address on the common bus (page 6, lines 5-40, since the processor #1 has send the access information to common bus, if the semf-a is busy the access information remains on the bus to snoop data read by processor #0).

As per claims 3, and 8, AAPA teaches when access to a prescribed data area in said common memory is requested by a host apparatus, the access controller of each processor reads control information corresponding to this data area in said storage unit determines whether another processor is busy and if another processor is busy, inputs result of the determination to the host apparatus without accessing said common memory (pages 6-7, lines 27-3).

As per claim 4, AAPA teaches when read-out of data from a prescribed data area in said common memory is commanded by a host apparatus, said data area in said storage unit is valid, then the access controller of a processor that has access privilege reads data from this data area and inputs the data to the host apparatus (pages 3-4, lines 35-26).

As per claim 5, AAPA teaches writing of data to a prescribed data wherein when area in said common memory is commanded by the host apparatus, the access controller of a processor that has access privilege writes data to a data area of said

storage unit and sends this data as well as an address corresponding to this data area to the common bus (pages 4-5, lines 23-8).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mehdi namazi
3/30/2007

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